Attorney Docket No.: 5649-1098 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Moon et al.
Serial No.: 10/715,015
Filed: November 17, 2003
For: VARIABLE-DELAY PRECHARGE CIRCUITS AND METHODS

Group Art Unit: 2824
Examiner: Jung H. Hur
Confirmation No.: 3312

September 13, 2007

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Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' REPLY TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Sir:

This paper is filed pursuant to the "Notification of Non-Compliant Appeal Brief" mailed August 15, 2007.

It is not believed that an extension of time and/or additional fee(s) are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. Sec. 1.136(a). Any additional fees believed to be due may be charged to Deposit Account No. 50-0220.

Appellant provides the following revised "Summary of Claimed Subject Matter" to overcome the objections in the "Notification of Non-Compliant Appeal Brief " mailed August 15, 2007.

Summary of Claimed Subject Matter

According to independent Claim 1, a memory device includes a data line (see, e.g., FIG. 2, reference IO, IOB) and a variable delay precharge circuit (*see, e.g.*, FIG. 2, reference 2000) that receives a column bank address signal (see, e.g., FIG. 2, reference CBA) and a write enable signal (see, e.g., FIG. 2, reference PWR) and that precharges the data line responsive to the column bank address signal at a time that is determined by a state of the write enable signal. The variable delay precharge circuit includes a precharge circuit (*see, e.g.*, FIG. 2, reference 250) operative to precharge the data line responsive to a precharge control signal (see, e.g., FIG. 2-4, reference PIOPRB1, PIOPRB2). The variable delay precharge circuit also includes a precharge control signal generator circuit (*see, e.g.*, FIG. 2, reference 200) that receives the column bank address signal, that generates first and second delayed signals (*see, e.g.*, FIG. 2, reference I45Z and I10Z) from the column bank address signal that are delayed by respective different first and second time periods with respect to the column bank address signal, and that applies to the precharge circuit, responsive to a precharge delay control signal (*see, e.g.*, FIG. 2, reference IOPREFNB), a selected one of a first precharge control signal (*see, e.g.*, FIG. 3, PIOPRB1) generated from the first delayed signal and a second precharge control signal (*see, e.g.*, FIG. 4, PIOPRB2) generated from the second delayed signal. The variable delay precharge circuit further includes a precharge delay control circuit (*see, e.g.*, FIG. 2, reference 210) that generates the precharge delay control signal responsive to the write enable signal. *See, e.g.*, circuit description at specification, p. 5, line 11, through page 6, line 34, and operational description at specification, p. 7, line 1 through page 8, line 16.

According to independent Claim 6, a memory device includes a pair of data input/output lines (see e.g., FIG. 2, reference IO, IOB) and a precharge circuit (*see, e.g.*, FIG. 2, reference 250) that precharges the pair of data input/output lines responsive to a precharge control signal (see, e.g., FIG. 2-4, reference PIOPRB1 and PIOPRB2). The memory device also includes a precharge control signal generator circuit (*see, e.g.*, FIG. 2, reference 200) that receives a column bank address signal (see, e.g., FIG. 2, reference CBA), that generates first and second delayed signals (*see, e.g.*, FIG. 2, reference I45Z and I10Z)

from the column bank address signal that are delayed by respective different first and second time periods with respect to the column bank address signal, and that applies to the precharge circuit, responsive to a precharge delay control signal (*see, e.g.*, FIG. 2, reference IOPREFNB), a selected one of a first precharge control signal (*see, e.g.*, FIG. 3, PIOPRB1) generated from the first delayed signal and a second precharge signal (*see, e.g.*, FIG. 4, PIOPRB2) generated from the second delayed signal. The memory device further includes a precharge delay control circuit (*see, e.g.*, FIG. 2, reference 210) that generates the precharge delay control signal responsive to a write enable signal (see, e.g., FIG. 2, reference PWR). *See, e.g.*, circuit description at specification, p. 5, line 11, through page 6, line 34, and operational description at specification, p. 7, line 1 through page 8, line 16.

According to independent Claim 9, a precharge control circuit for controlling a precharge circuit (*see, e.g.*, FIG. 2, reference 250) of a semiconductor memory device includes a precharge control signal generator circuit (*see, e.g.*, FIG. 2, reference 200) that receives a column bank address signal (see, e.g., FIG. 2, reference CBA), that generates first and second delayed signals (*see, e.g.*, FIG. 2, reference I45Z and I10Z) from the column address bank signal that are delayed by respective different first and second time periods, and that applies, responsive to a precharge delay control signal (*see, e.g.*, FIG. 2, reference IOPREFNB), a selected one of a first precharge control signal (*see, e.g.*, FIGs. 2 and 3, reference PIOPRB1) generated from the first delayed signal and a second precharge control signal (*see, e.g.*, FIGs. 2 and 4, reference PIOPRB2) generated from the second delayed signal. The precharge control circuit further includes a precharge delay control circuit (*see, e.g.*, FIG. 2, reference 210) that generates the precharge delay control signal responsive to a write enable signal (see, e.g., FIG. 2, reference PWR). The precharge delay control circuit causes application of the first precharge control signal after a read operation of the memory device and application of the second precharge control signal after a write operation of the memory device.

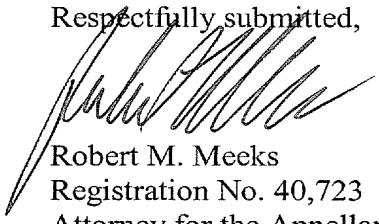
According to independent Claim 15, methods of generating a precharge control signal for a precharge circuit (*see, e.g.*, FIG. 2, reference 250) of a memory device include receiving a column bank address signal (see, e.g., FIG. 2, reference CBA), generating a first delayed signal and a second delayed signal (*see, e.g.*, FIG. 2, reference I45Z and I10Z) from the column bank address signal that are delayed respective first and second time periods, and selectively generating the precharge control signal from one of the first delayed signal or the second delayed signal based on a state of a write enable signal (*see, e.g.*, FIG. 3, PIOPRB1

and FIG. 4, PIOPRB2). The first time period is greater than the second time period. *See*, *e.g.*, circuit description at specification, p. 5, line 11, through page 6, line 34, and operational description at specification, p. 7, line 1 through page 8, line 16.

Conclusion

Appellants submit that the Summary provided herein overcomes the deficiencies alleged in the Notification of Non-Compliant Appeal Brief. Appellants request consideration of the remarks herein and in the Appeal Brief filed June 19, 2006, and reversal of the rejections of Claims 1, 4-10, 15 and 16.

Respectfully submitted,



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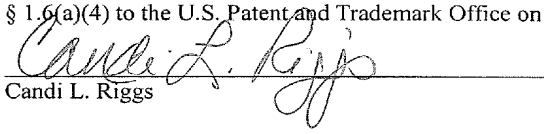

Candi L. Riggs